

Parallel Implementation Of Clutter Suppression Of Passive Radar Based On LDLT

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I. INTRODUCTION

Passive radar is a bistatic radar, which has attracted extensive attention over the world. The signal received by passive radar is always disturbed by clutter interference. At present, the mainstream clutter cancellation algorithm of passive radar is the extensive cancellation algorithm batches (ECA-B). How to improve the real-time processing performance of ECA-B algorithm is a key step in the passive radar target realtime tracking sys. This paper proposed an innovative method that improves the effectiveness of ECA-B algorithm by segmented parallel processing, which is combined with the same sub-module characteristics of each segment based on GPU multithreading parallel processing technology. The cost of the time of data transmission in the inversion process of traditional ECA-B algorithm is economized by proposing a parallel iterative inversion method based on LDLT leveraging.

II. ECA-B ALGORITHM

Suppose the received signal of the reference channel is $S_{ref}(t)$, the target echo signal is $S_{sur}(t)$, and the transmitter signal is $S(t)$.

$$S_{ref}(t) = s(t - \tau) + n_{ref}(t) \quad (1)$$

$$S_{sur}(t) = \sum_{k=1}^K \alpha_k s(t - \tau_k) e^{j2\pi f_k t} + \sum_{i=0}^M \beta_i s(t - \tau_i) + n_{surv}(t) \quad (2)$$

The sliding matrix formed by the h-segment reference signal is:

$$V_h = \begin{bmatrix} S_{ref}(1) & S_{ref}(2) & \dots & S_{ref}(C) \\ S_{ref}(2) & S_{ref}(3) & \dots & S_{ref}(C+1) \\ \vdots & \vdots & \ddots & \vdots \\ S_{ref}(H) & S_{ref}(H+1) & \dots & S_{ref}(H+C) \end{bmatrix} \quad (3)$$

The residual signal of H segment is obtained by subtracting the product of the sliding matrix of H segment and the weight vector from the echo signal of H segment, which is shown as

$$S_{rem,h} = S_{sur,h} - V_h W_h = S_{sur,h} - V_h (V_h^H V_h)^{-1} V_h^H S_{sur,h} \quad (4)$$

III. Improvement and parallel implementation of algorithm

A. Piecewise parallel implementation of ECA-B algorithm

This paper uses thread index to control each thread to access data at a specific location in global memory, when writing kernel functions with CUDA. The same calculation links in the process are put together for calculation, and the calculation links of different segments are calculated independently with thread blocks. The algorithm implementation process is shown in Fig. 1. For example, calculate R_h as an example, the thread network allocates h thread blocks, and each thread block opens up C threads. h thread blocks correspond to calculate the R_h in the hth segment of ECA-B algorithm. The algorithm implementation process is shown in Fig. 2, computing matrices C_h , D_h , V_h and S_h are the same.

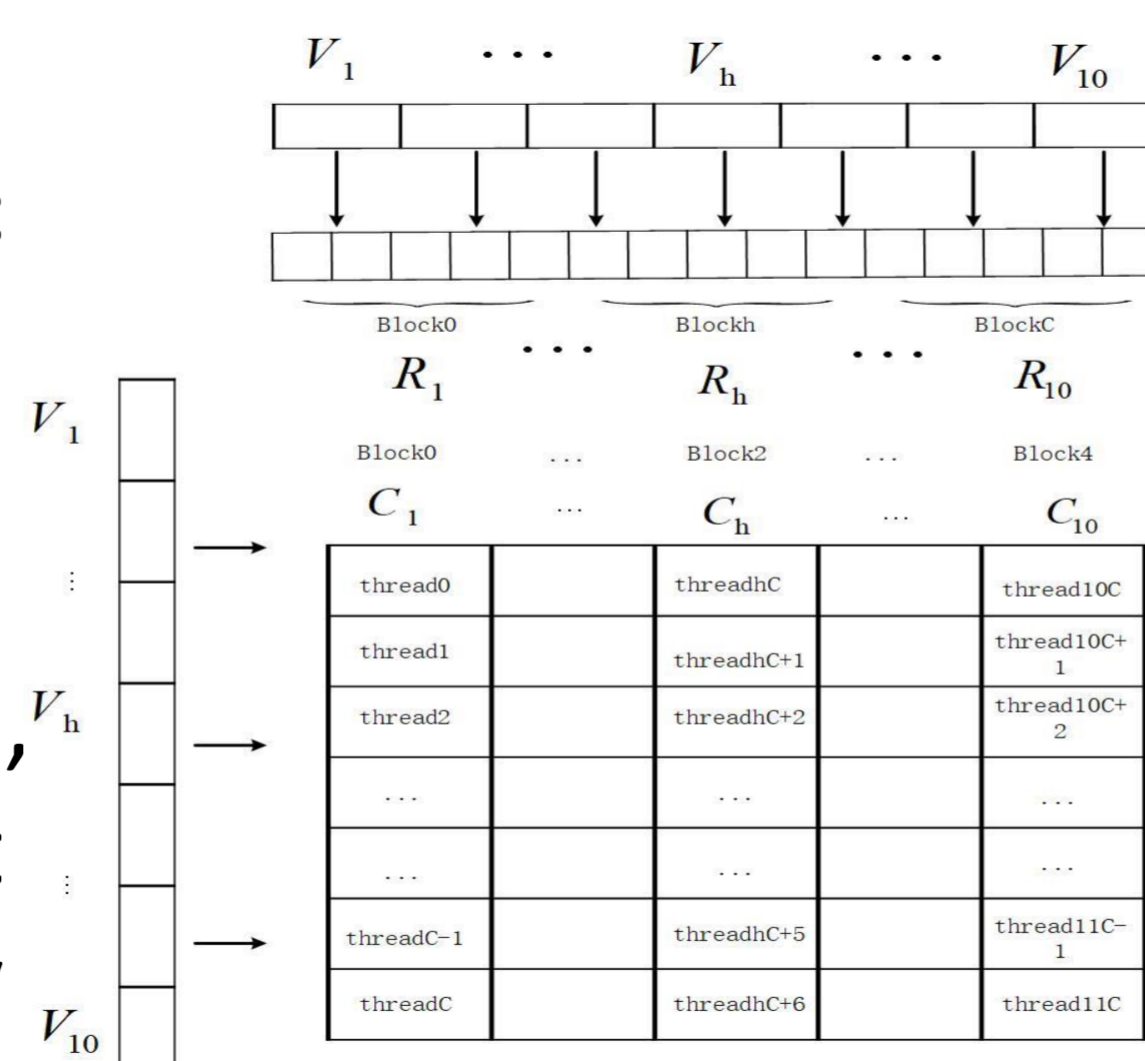


Fig.1. Schematic diagram of GPU calculation R and C

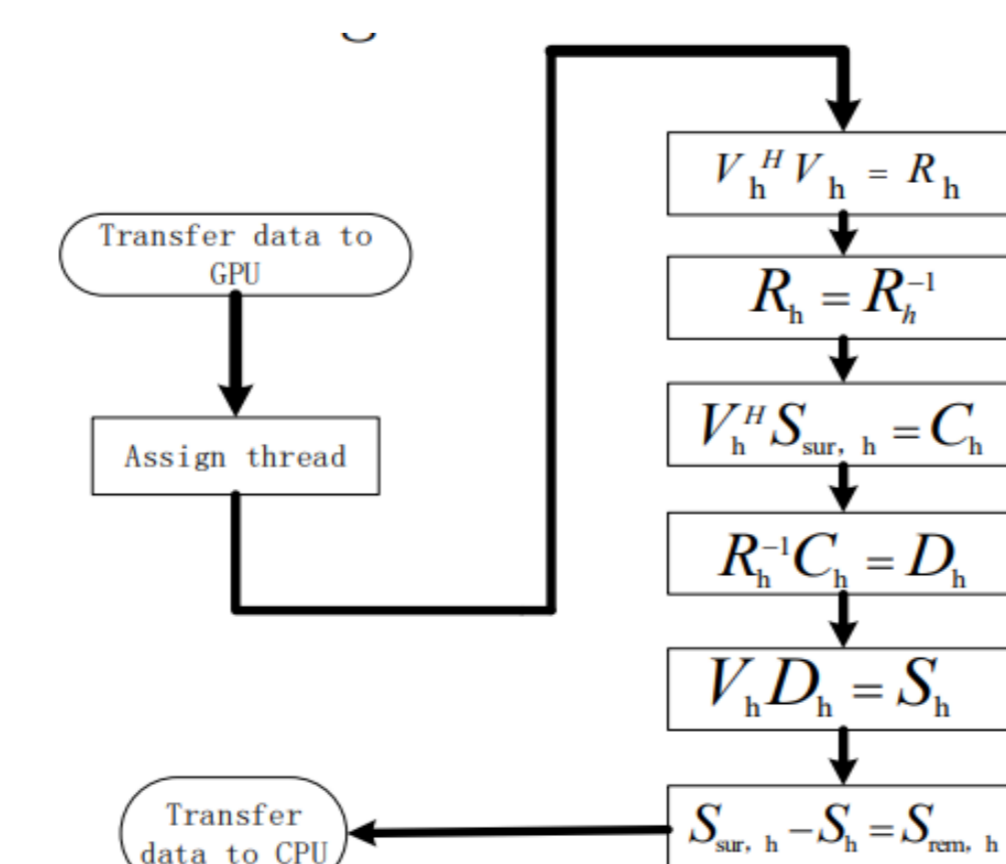


Fig.2. Flow chart of algorithm program implementation

B. LDLT decomposition inversion

This paper adopts LDLT decomposition method, which is improved by Cholesky decomposition method. In this paper, two GPU kernel functions are used to inverse the matrix. By normalizing the column vectors of the triangular matrix L of the Cholesky decomposition method, an improved Cholesky decomposition form can be obtained, i.e., $A = LDL^H$. According to the definition of inverse matrix $LB = E$, the inverse matrix of matrix L can be derived, and the formula is as follows:

$$b_{ij} = -\sum_{k=j}^{i-1} l_{ik} b_{kj} \quad (5)$$

the LDLT decomposition method can be implemented in parallel iterations.

IV. PERFORMANCE TESTING

In order to verify the clutter suppression effect of the proposed algorithm, CPU and GPU are used for clutter elimination respectively, and the results are shown in the figure below. Fig.3 is the range Doppler spectrum of the signal clutter suppression by CPU. Fig. 4 shows the range Doppler spectrum of clutter suppression by GPU. It can be seen that the results in Fig. 3(a) and Fig. 3(b) are almost the same, and the range Doppler spectrum of the target is obtained. The results of speedup ratio in different orders are shown in Table (I). The maximum speedup ratio is 3.5 times, which greatly shortens the operation time of the algorithm. The larger the cancellation order, the more data will be processed. Besides, it can be seen that the increase of cancellation order has a small impact on the inter segment parallel algorithm and a large impact on the inter segment serial algorithm in file [11]. This shows that the inter segment parallel algorithm proposed in this paper has good time performance.

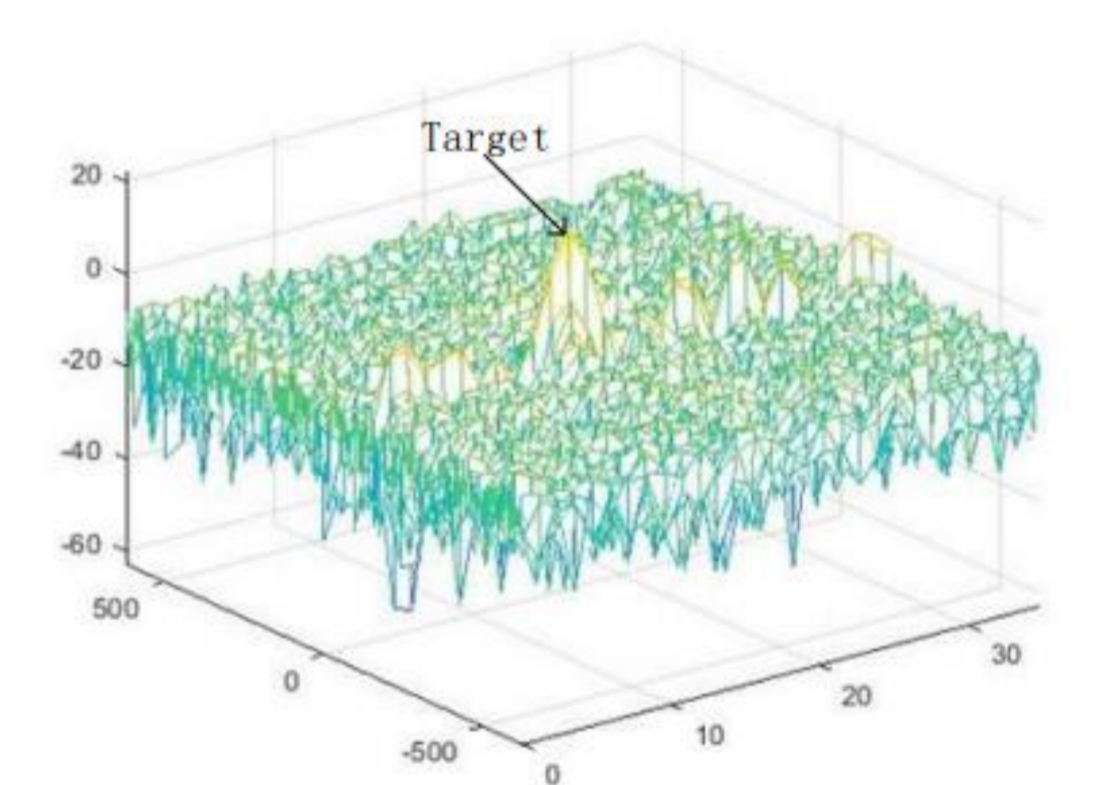


Fig. 3. CPU clutter suppression range Doppler spectrum

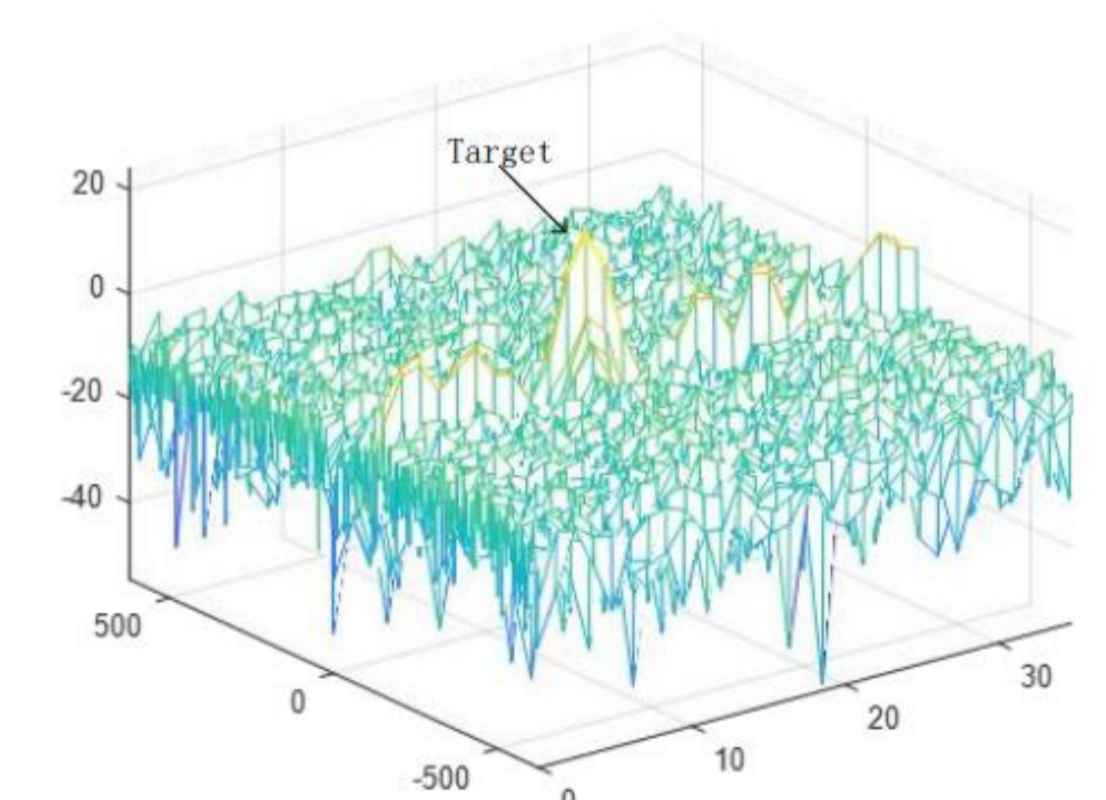


Fig. 3. GPU clutter suppression range Doppler spectrum.

TABLE I
Comparison of clutter suppression experimental results.

Canlation order	Algorithm in this paper/ms	Literature [16] algorithm/ms	Acceleration ratio
48	12	23.5	1.95
64	16	34	2.12
128	45	81	1.8
144	56	99	1.7
176	103	196	1.9
192	121	410	3.2
224	176	627	3.5

ACKNOWLEDGMENT

This work is partially supported by Guangxi special fund project for innovation-driven development ffGuikeAA21077008ffffGuangxi science and technology base and talent project(AD20297038), Research project on basic ability of young and middle aged teachers in Guangxi(2021KY0197)

