Design and Implementation of Broadband Satellite IF Transceiver

Dongsong Li [1], Xueya Dai[2], Peng Chen[1], Xutao Yu[1], Zeng Rong[3]
[1]State Key Laboratory of Millimeter Waves, Southeast University.
[2]Nanjing Panda Handa Technology Co., Ltd.
[3]National Mobile Communications Research Laboratory, Southeast University

毫米波国家重点实验室
State Key Laboratory of Millimeter Waves

Background

- **Since the 1980s, zero-IF structure has gradually been widely used, the volume is much smaller than that of the superheterodyne.**
- **With the development of semiconductor technology, zero-IF structure has been further studied and applied .**
- **However, for a zero-IF transceiver, the imbalance of the I/Q channel will produce an image frequency at the zero frequency.**
- **Here we proposes a zero-IF transceiver composed of a 16-channel third-order Wilkinson power divider module. And it adopts the compensation correction of I/Q amplitude and phase imbalance to achieve a better image rejection ratio.**

Receiver Module & Transmitter Module

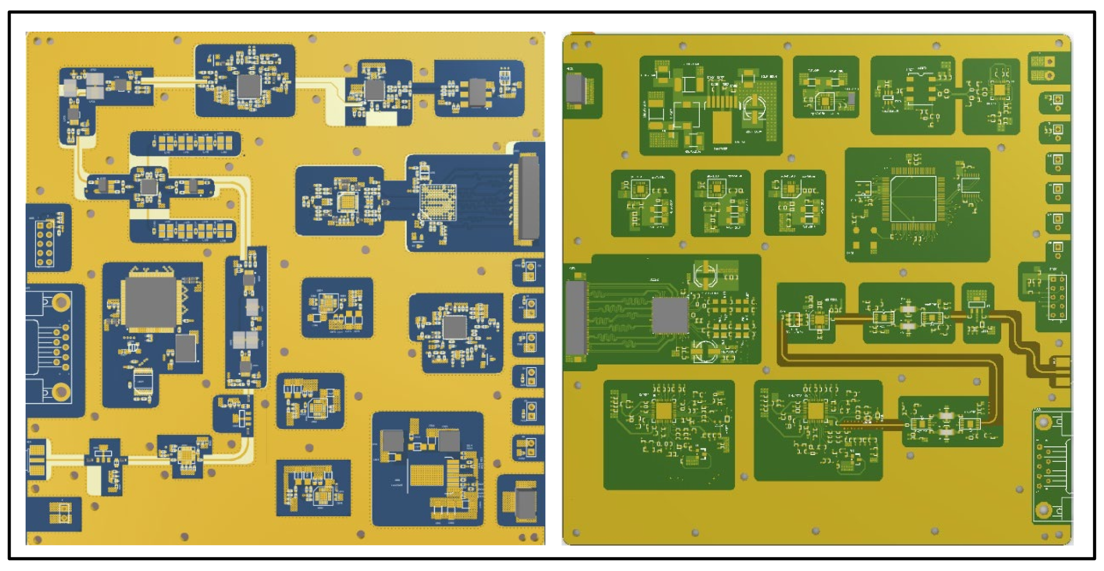
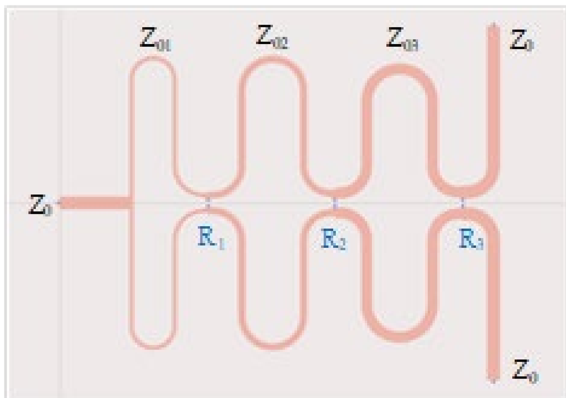


Figure 1 The complete PCB layouts of the receiver and transmitter IF system modules are shown in Fig. 1. IF system consists of ADC/DAC module, modulation and demodulation module, control module, power module, clock module and other parts.

Design of Power Divider



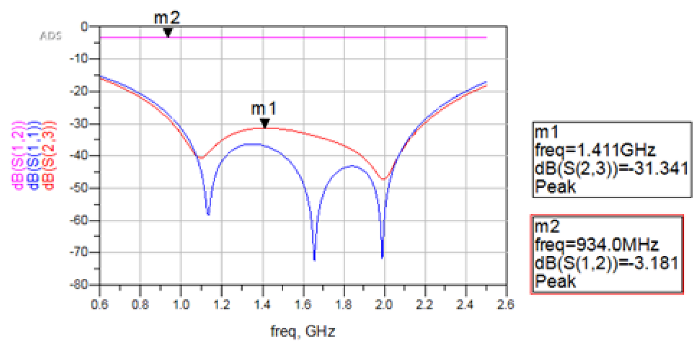


Figure 2 layout of divider

Figure 3 S-parameter of divider

Implementation of Power Divider

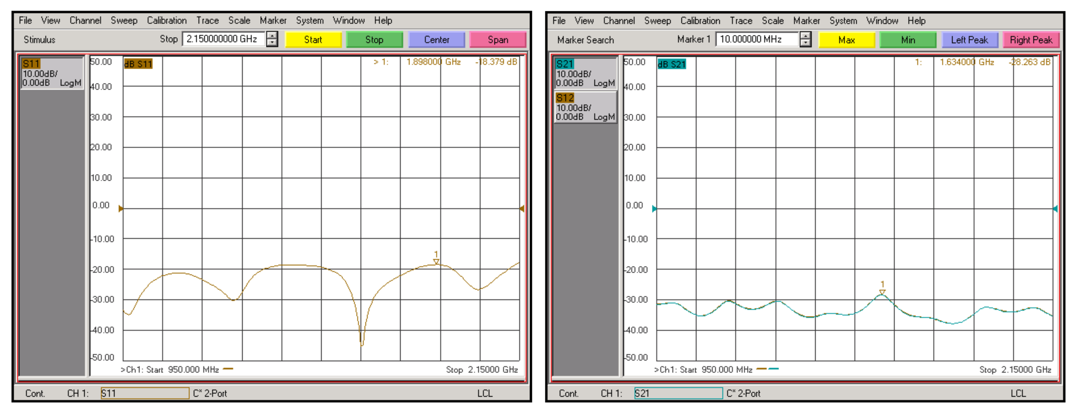


Figure 4 fabrication of divider.

Figure 5 reflection of divide & isolation of divider

Transmitter Schematic Design & Receiver Schematic Design

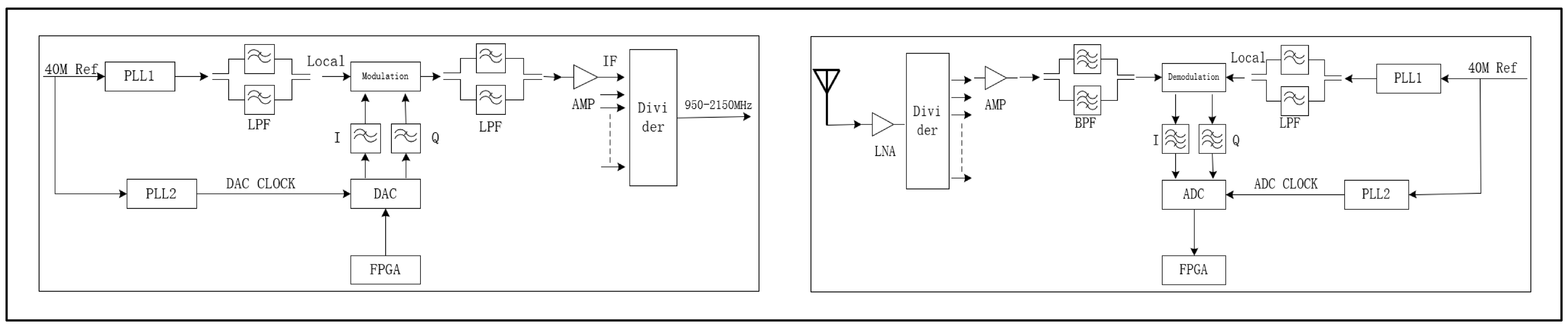


Figure 6 For transmitter, FPGA module generates IQ digital baseband signal and sends it to dual-channel DAC through FMC switching module. DAC converts digital IQ signal to analog IQ baseband signal, and passes through LC baseband anti-image filter. After filtering the Nyquist image and broadband DAC noise, the signal is sent to the input of the quadrature modulator, and is modulated to 950-2150MHz. After the signal passes through the switch filter bank to filter out high-order harmonics, the signal is amplified by the amplifier to obtain the required IF signal. The select modulation chip is ADL5375 from Analog Devices. ADL5375 is a wideband quadrature modulator with a working frequency range of 400MHz-6GHz.

Fabrication of receive and transmitter

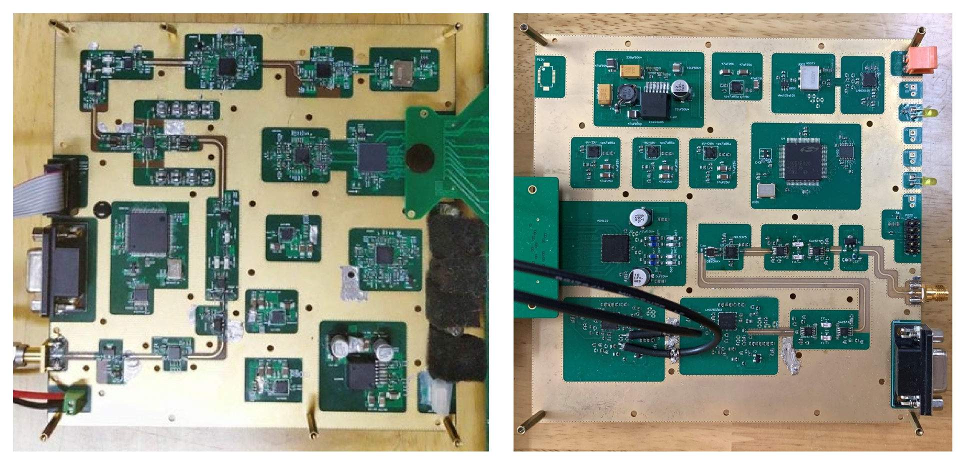


Figure 7 The IF transceiver circuit board uses an 8-layer epoxy resin (FR4) board with a dielectric constant of 3.95 and the thickness of FR4 is 0.25mm. The adhesive layer uses 2116pp sheets with a thickness of 0.131mm. The total thickness of the PCB is about 1.2mm.

The IRR of transmitter

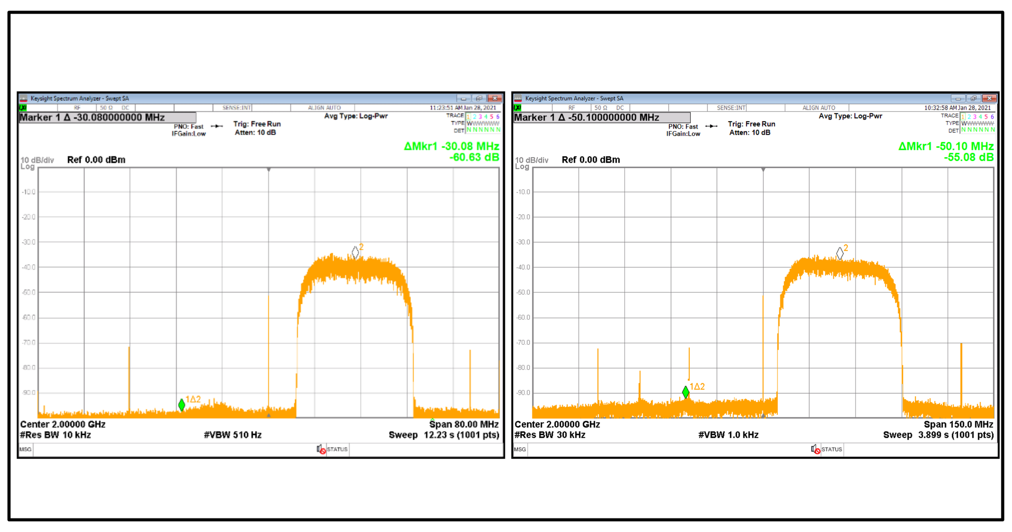


Figure 8 For the transmitter, when the local oscillator frequency is 2GHz, the FPGA generates a QPSK signal with a code rate of 15Msps, the IRR is 60.63dBc. When the symbol rate is 30Msps, the IRR is 55.08dBc.

The IRR of receiver

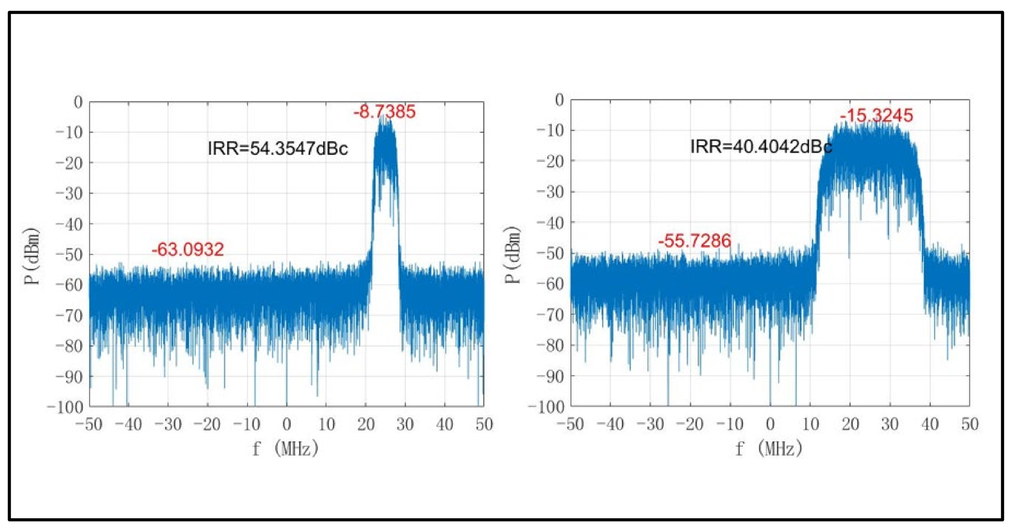


Figure 9 For the receiver, when the local oscillator frequency is 1.925GHz and the code rate of QPSK signal is 5Msps, the IRR is 54.4dBc. When the code rate of QPSK signal is 20Msps, the IRR is 40.4dBc.

The EVM of transmitter and receiver

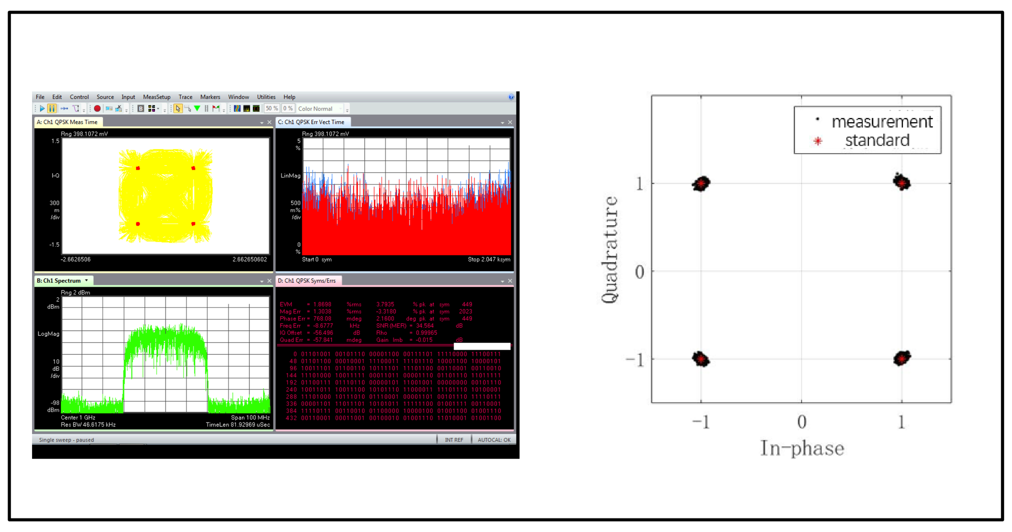


Figure 10 For the transmitter, select the 1GHz carrier to measure the modulation accuracy of the IF signal, the FPGA generates a QPSK signal with a code rate of 30Msps, the EVM is 1.87%. For the receiver, select the 1.9GHz carrier. For the QPSK signal with a code rate of 20Msps, the EVM is 2.81%.

Conclusions

A broadband IF subsystem used in Ku-band satellite transceiver is designed and implemented in this work. By adopting I/Q amplitude and phase imbalance calibration, the measured results show a good image frequency rejection. The proposed IF transceiver has excellent IRR and EVM, which can be utilized in the broadband satellite communication systems.

References

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