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Design and Implementation of CNN Traffic Lights Classification Based on FPGA

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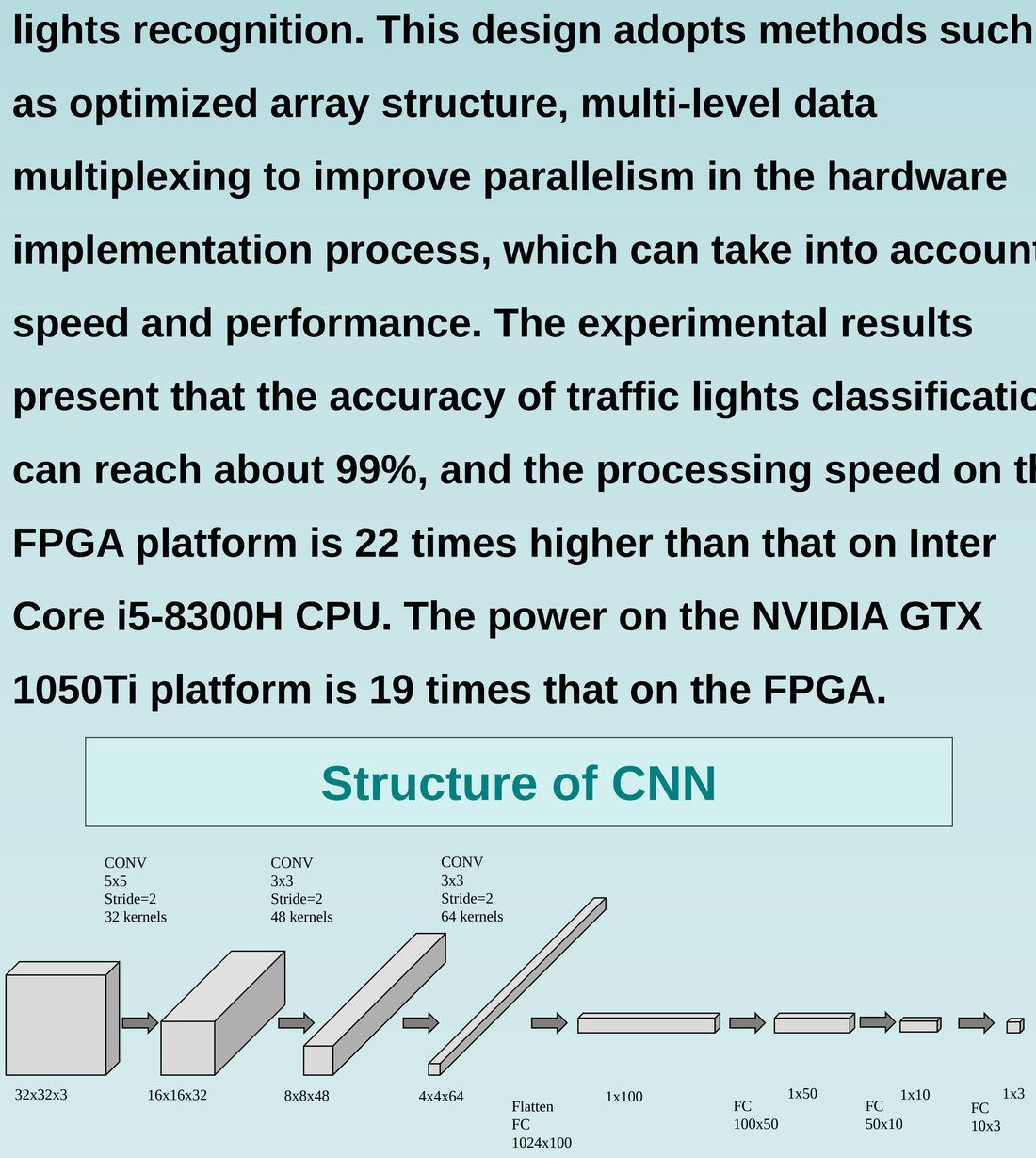
Abstract

This paper proposes a tri-classification convolutional neural networks with a simple structure and easy FPGA implementation, which is used to realize traffic lights recognition. This design adopts methods such as optimized array structure, multi-level data multiplexing to improve parallelism in the hardware implementation process, which can take into account speed and performance. The experimental results present that the accuracy of traffic lights classification can reach about 99%, and the processing speed on the FPGA platform is 22 times higher than that on Inter Core i5-8300H CPU. The power on the NVIDIA GTX 1050Ti platform is 19 times that on the FPGA.

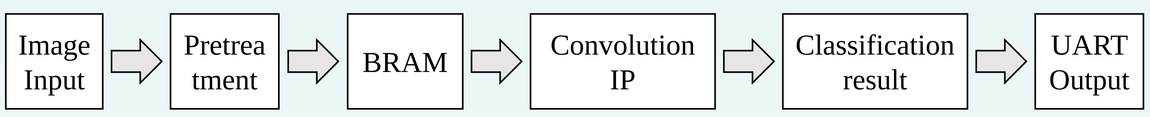
Structure of CNN



The same training dataset is used to train the improved CNN (convolution step size is two) and classic CNN (convolution step size is one and maximum pooling), and the number of parameters trained by the two networks is the same. In this case, the accuracy of the improved CNN is 3% higher than that of the classic CNN, and the amount of computation is only 28% of that of the classic CNN. Obviously, the performance of the improved CNN is better.

Methods

Hardware structure flow chart

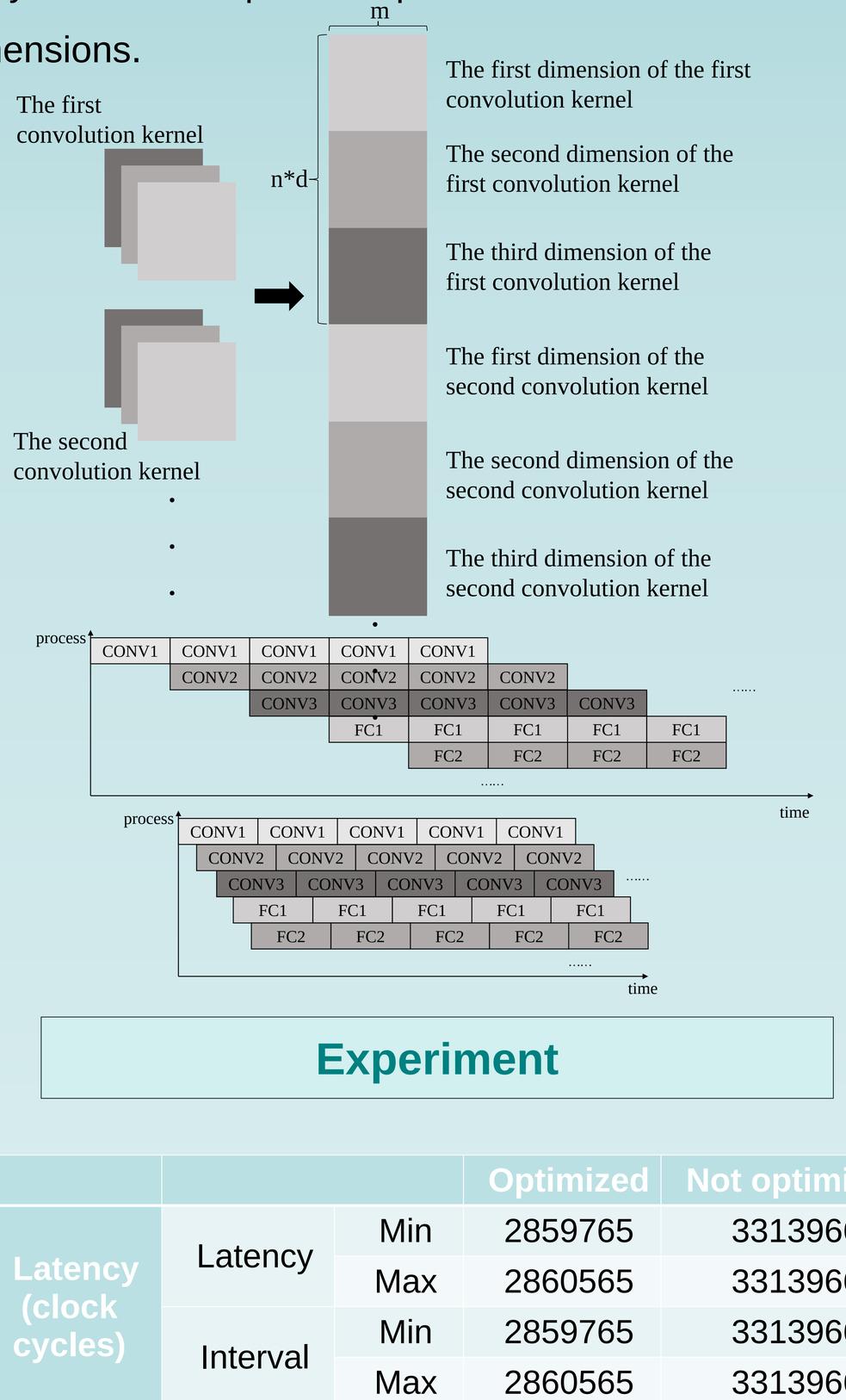


Curing parameters

The weight and bias parameters are stored as static variables. Its advantage is that the static variables have been written into the bitstream file during the compilation process.

Optimization and multiplexing of arrays

This design converts the weight parameters in the form of high-dimensional arrays into the form of two-dimensional arrays to facilitate parallel operations between different dimensions.



Experiment

			Optimized	Not optimized
Latency (clock cycles)	Latency	Min	2859765	3313966
		Max	2860565	3313966
	Interval	Min	2859765	3313966
		Max	2860565	3313966
Utilization Estimates	BRAM_18K		23	283
	DSP48E		21	26
	FF(Flip-Flop)		3728	4683
	LUT		4962	6223

Conclusion

This design transplants the improved CNN to FPGA in a low-cycle and high-efficiency way and makes full use of the parallelism of FPGA. It is not sensitive to the number of convolutional layers and the size of weight parameters, so it can be widely applied to the transplantation of convolutional neural networks. This design has great significance to the engineering achievement of neural networks.