Design of Distributed Ultra-high-definition Resolution Display System

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***Abstract*—A practical and scalable ultra-high-definition resolution display system for multi-screen display wall is constructed based on multiple distributed low-definition display nodes, and the collaborative processing mechanism between distributed display nodes is the key to the performance of the display system. In order to improve the performance of image synchronization between distributed nodes, a node collaboration mechanism based on IEEE1588 time synchronization protocol and phase-locked loop is proposed. A synchronization processing system applied to ultra-high-definition resolution displays is designed, which not only shortens the image processing time but also improves the image synchronization processing performance. The system synchronization test results show that the maximum display frame difference between splicing display units is 0.47 frame and the average system delay is 98.67ms. The provided system can effectively shorten system data processing time, solve synchronization problems of ultra-high-definition resolution displays, meet requirements of large screen display images, and improve users' experience effect.**

Keywords—distributed, ultra-high-definition resolution, system synchronization, system delay

Ⅰ ULTRA-HIGH-DEFINITION RESOLUTION DISPLAY SYNCHRONIZATION PROCESSING SCHEME

In order to further improve the efficiency of video processing in ultra-high-definition resolution display systems, the original video stream is often divided into blocks through a blocking module and sent to encoding nodes 1, 2,... , and N for encoding processing. Then, they are converted by the switch to corresponding decoding nodes for parallel processing, splicing, and displaying. The distributed signal processing framework is shown in Fig.1.

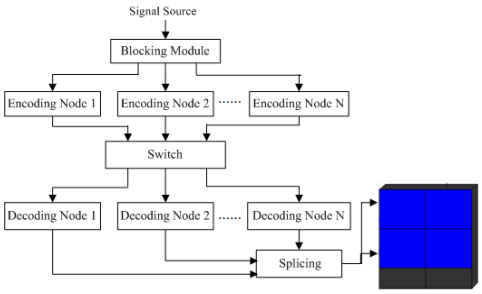

Fig.1. The distributed signal processing framework for ultra-high-definition resolution display system

Using the IEEE1588 time synchronization protocol [6][7] to solve the problems of delay and synchronization, the best performing crystal oscillator clock source node is designated as the primary clock, and the timing and path delay estimation of the primary and secondary clocks are completed through the precise timestamp of synchronous message communications. The delay response mechanism process is shown in Fig.2.

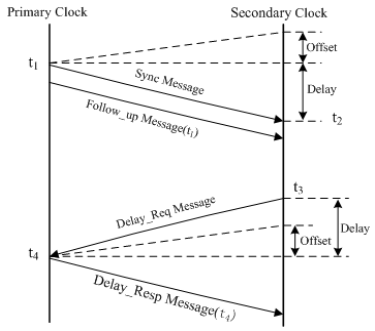

Fig.2. Delay response flowchart of IEEE 1588 time synchronization protocol

Using the four timestamp, information, the primary and secondary clock offset and transmission delay can be attained, as shown by Equation (1) and (2).

$$Offset = \frac{(t_2 - t_1) - (t_4 - t_3)}{2} \quad (1)$$

$$Delay = \frac{(t_2 - t_1) + (t_4 - t_3)}{2} \quad (2)$$

Ⅱ SYSTEM DESIGN AND EXPERIMENTAL RESULTS

A. Distributed ultra-high-definition resolution display synchronization processing system

A distributed ultra-high-definition resolution display synchronization processing system has been designed based on the concept of distributed processing, which consists of four parts: customer control platform, display platform, control exchange platform, and signal acquisition platform, as shown in Fig.3.

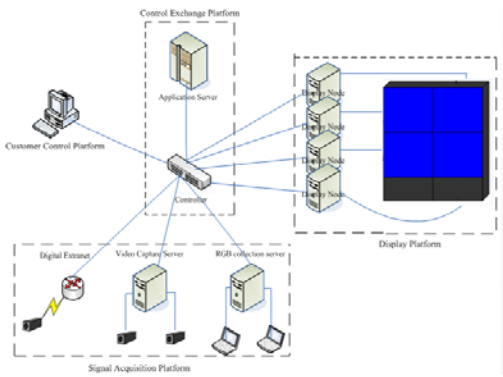

Fig.3. The distributed ultra-high-definition resolution display synchronization processing system

B. System performance testing

In order to determine the performance of the system, the testing standards and software of GA/T1084-2020 "General specification for large activity mosaic display systems" are used to measure system synchronization and delay.

1) System synchronization

The system synchronization refers to the maximum display frame difference when displaying the same signal source test video between each splicing display unit.

a) Input 1-channel 60Hz video signal and play the running electronic millisecond meter in the video content.

b) According to the screen size, each unit opens the same 1-channel signal window. In this experiment, four display units are selected, and the signal source of the graphics card is configured with four clones to output to the four display units, and the 4-channel signal window of the display unit is opened.

c) Record the millisecond meter readings of the signal display window on each unit in the imaging photo taken by a high speed camera equipment, as shown in Fig.4. The detailed test data is shown in Table Ⅰ. The maximum display frame difference can be attained by calculating maximum millisecond difference of the signal between any units.

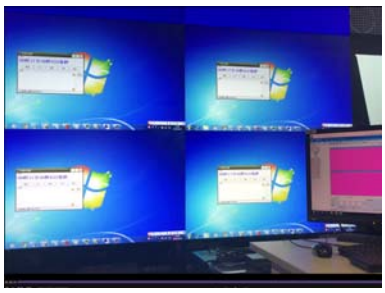

Fig.4. Millisecond meter readings of signal display window on each unit

TABLE Ⅰ. MILLISECOND METER READINGS OF SIGNAL DISPLAY WINDOWS ON EACH UNIT
(The video recording frame rate is 30FPS, unit: seconds)

DISPLAY UNIT	The 1st unit	The 2nd unit	The 3rd unit	The 4th unit
The 1st test	25.578	25.546	25.573	25.568
The 2nd test	27.248	27.233	27.248	27.248
The 3rd test	30.432	30.432	30.432	30.432
Average results	27.75267	27.737	27.751	27.74733
Delay results (Compared with the 1st unit)	0	-0.01567	0.00167	0.00534

It can be seen that the maximum difference between the 4 channels is 15.67 milliseconds, which can be converted into the maximum display frame difference. Therefore, the maximum display frame difference between system synchronization splicing display units is 15.67 * 30/1000 =0.47 frame.

2) System Delay

The system delay refers to the maximum processing time required for the input video signal from entering the splicing display system to reaching its display output. It reflects the real-time processing performance of the system.

a) Prepare one 60Hz video signal and run an electronic millisecond meter during video content playback.

b) Distribute the above video signal into two outputs through a 1/2 distributor. One output connects to a local source LCD display, and the other connects to the input end of the splicing display wall system. The entire multi-screen display wall displays the above input source video signal on a full screen.

c) Use camera equipment to simultaneously take high-speed photos of the local LCD display and the multi-screen display wall, record the millisecond meter readings on the imaging photos. The system delay can be attained by calculating the millisecond difference Δ T between the local LCD display and the multi-screen display wall. The experimental data is shown in Table Ⅱ.

TABLE Ⅱ. MILLISECOND METER READINGS OF LCD DISPLAY AND THE MULTI-SCREEN DISPLAY WALL
(UNIT: SECONDS)

Display types	The 1st test	The 2nd test	The 3rd test
LCD display	41.426	41.737	42.907
Multi-screen display wall	41.316	41.644	42.814
Individual different results	0.110	0.093	0.093
Average different result	0.09867		

The system delay can be taken by the average delay millisecond difference ΔT=98.67 milliseconds of three test results.

The above experimental results indicate that the proposed method has significant improvements in both system synchronization and system delay.

Ⅲ CONCLUSION

This article designs a synchronization processing system for ultra-high-definition resolution displays based on the IEEE1588 time synchronization protocol and the node collaboration mechanism of phase-locked loops. According to the testing methods and software provided in the GA/T 1084-2020 standard, the test results show that the distributed ultra-high-definition resolution display system designed in this paper achieves excellent performance. The maximum display frame difference obtained from system synchronization testing between splicing display units is 0.47 frame, and the average system delay is 98.67ms. This effectively shortens the system data processing time, solves the synchronization problems, and improves the users' experience.